X BAND INTEGRATED DIODE PHASE SHIFTERS

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Recent advances in solid state microwave technology have made possible the fabrication of diode phase shifters in hybrid integrated circuit form. However, work at X band has been hindered by the limited isolation presently available with diodes at this frequency. Actually, accurate phase shifters can still be built if one accounts for this limited isolation in the design and analysis of the systems. This paper outlines this analysis and applies it in the design of low insertion loss phase shifters for wideband operation around 9 GHz. Surface oriented P^+IN^+ diodes are used in these switched line length systems to obtain phase shifts of up to 360°.

In a switched line length phase shifter two alternate paths between the input and output are available, each having a different length and phase delay. Four of the P^+IN^+ diodes are used per bit to change the attenuation factor through each of the parallel paths. The two diodes at each end of the isolated path are switched into the high impedance state to minimize power transmission through this path while the two diodes at each end of the preferred path are switched into the low impedance state to maximize power transmission through this path. As the diodes are switched back and forth, the overall phase delay shifts towards the value of the preferred path. An exact analysis of this effect is possible by setting up a flow graph model for the system.

I. Analysis and Design Procedure. The first requirement is to calculate the total effective impedance of each line at each junction in the system. The diodes are considered as lumped parameters concentrated at the junctions with diodes in the high impedance state appearing as capacitors and in the low impedance state appearing as inductors (Figure 1). The input and output lines are assumed to be terminated in matched loads. Starting at the output, the impedance at junction A is calculated using simple series-parallel combinations of the complex impedances assuming all to be lumped at this junction. The impedance is calculated looking in from each parallel path in the system terminating at that node. These impedances are then transformed along each path using a Smith Chart until junction B is reached. Here the transformed impedances are recombined in series and parallel assuming them to be lumped at this point. The impedance looking into junction B is calculated again for each parallel path terminating at this junction. This process is repeated until junction C, near the input of the device, is

reached and the effective impedance looking into each junction has been calculated.

Starting this time from the input and working towards the output, the power division at the junctions can be calculated by simple voltage division since all equivalent impedances are lumped together at the junctions. The effective voltage gain, A, through each path is determined by expressing the power flow through each path as a fraction of the input power:

$$A^2_{max} = \frac{\text{Power in Preferred Path}}{\text{Input Power}} \quad (1)$$

$$A^2_{min} = \frac{\text{Power in Isolated Path}}{\text{Input Power}} \quad (2)$$

A flow graph model can now be set up where each path is represented by a line with a value of phase delay and voltage gain (Figure 2). This flow graph can be reduced to an equivalent flow graph where the voltage at any node is determined by vector addition of all voltages in paths terminating at this node. This addition is shown in Figure 3 for a single phase bit. The results can be expressed in the general case as follows:

$$\text{Net Phase Shift} = \Delta\theta = \theta_1 - \theta_2 - 2 \arctan \frac{A_{min}}{A_{max}} \quad (3)$$

$$\text{Power Transmitted} = A_3^2 = [A_{max} + \cos(\theta_1 - \theta_2) A_{min}]^2 + [\sin(\theta_1 - \theta_2) A_{min}]^2 \quad (4)$$

where θ_1 and θ_2 are the values of phase delay through the two paths, and A_{max} and A_{min} are the effective voltage gains through each path in the maximized and minimized bias states respectively.

Given a design objective for the net phase shift, the nominal phase difference between the two paths can be calculated using equation (3). Realization of this value of the nominal phase difference $(\theta_1 - \theta_2)$ is achieved by using the proper length difference, Δx, between the two paths,

$$\Delta x = \frac{\theta_1 - \theta_2}{\lambda} \quad (5)$$

where λ is the wavelength of the microwave signal in the microstripline (0.40 times that of free space).

The total power transmitted through the system, A_3^2, can be maximized by designing each junction to look like a matched load seen from the preferred path. This reduces reflections and insures that all power not dissipated by the resistive losses is transmitted through the device.

II. Experimental Results. The first phase shifter was built with a nominal phase difference $\theta_1 - \theta_2 = 90°$ and used flip chip mounted P^+IN^+ diodes for switching (Figure 4). The impedance of these diodes in the high impedance state is capacitive at 90 Ω, and in the low impedance state is inductive at 2 Ω. Resistive losses are less than 1 Ω in both states. Using the impedance model (Figure 1), A_{min} was calculated at 0.40 and A_{max} at 0.89. Using Equation (3), a net phase shift of 42° was predicted. The net phase shift was measured directly to be 43° using a shorted termination and a slotted line.

The calculated junction impedances seen from the preferred path in this system were 40 Ω instead of the 50 Ω required for a matched load. This impedance mismatch is expected to yield a VSWR of 1.2 per junction or about 1.4 overall. The total measured VSWR varied between 1.40 and 1.55

Allowing only for reflections and diode losses, the power transmitted through the system, A_3^2, can be predicted using Equation (4). The predicted value of 0.87 is, of course, optimistic since it does not account for line losses, radiation losses, or internal reflections. The measured gain varied between 0.72 and 0.76.

This correlation between prediction and observation, while not perfect, is close enough to establish this method of analysis as useful in the design of integrated diode phase shifters where the effects of imperfect isolation are significant. Multibit phase shifters, such as the five bit device shown in Figure 5, have since been designed for use at S and X band frequencies.

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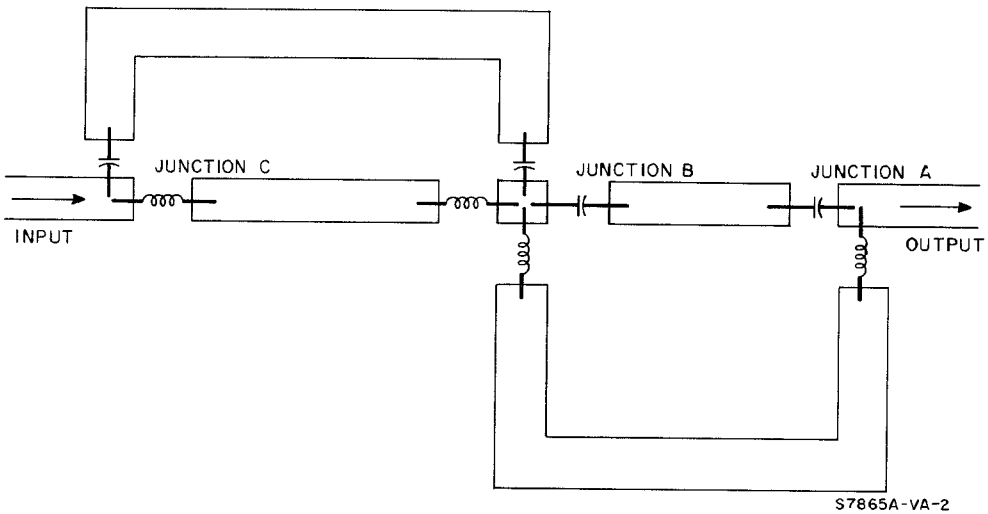

Figure 1. Impedance Model

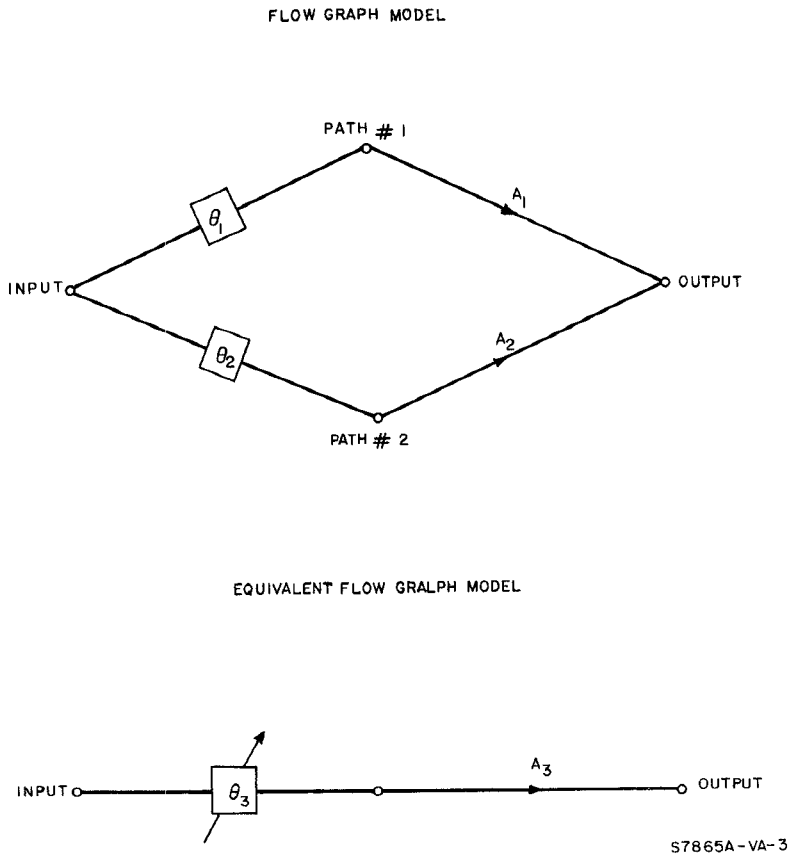

Figure 2. Flow Graph Analysis

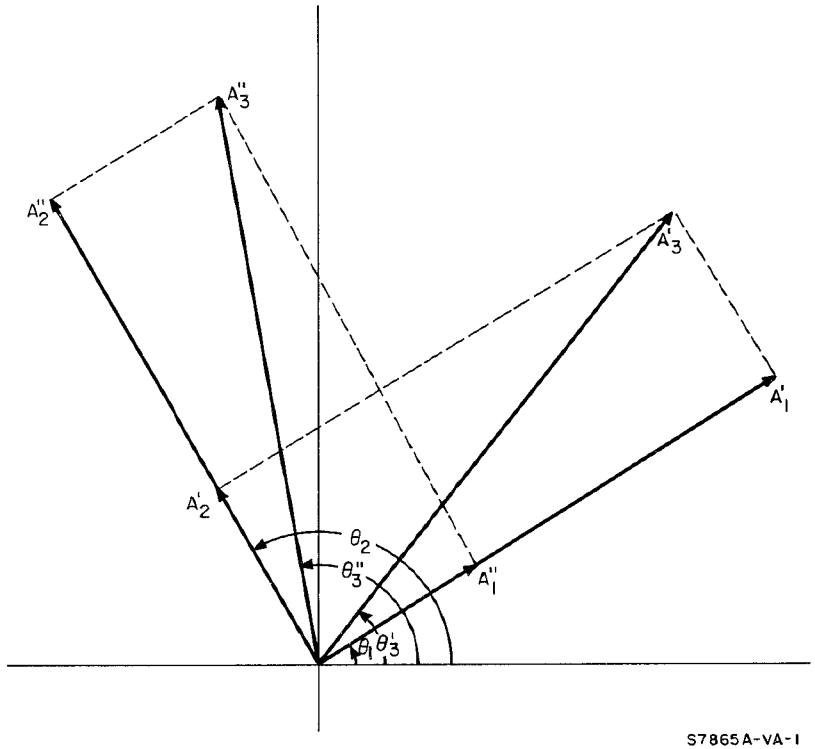

Figure 3. Vector Addition of Voltage Phasors

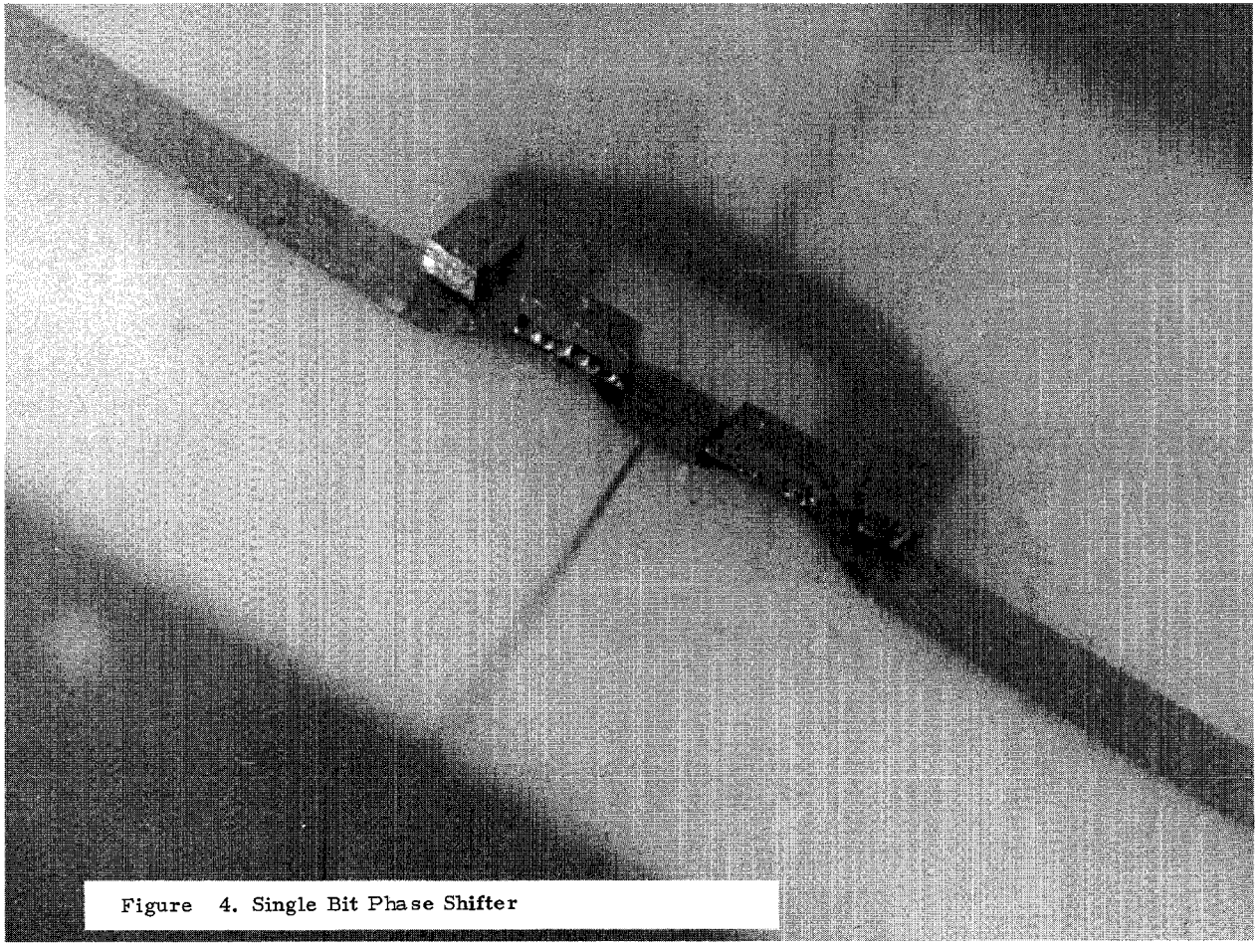

Figure 4. Single Bit Phase Shifter

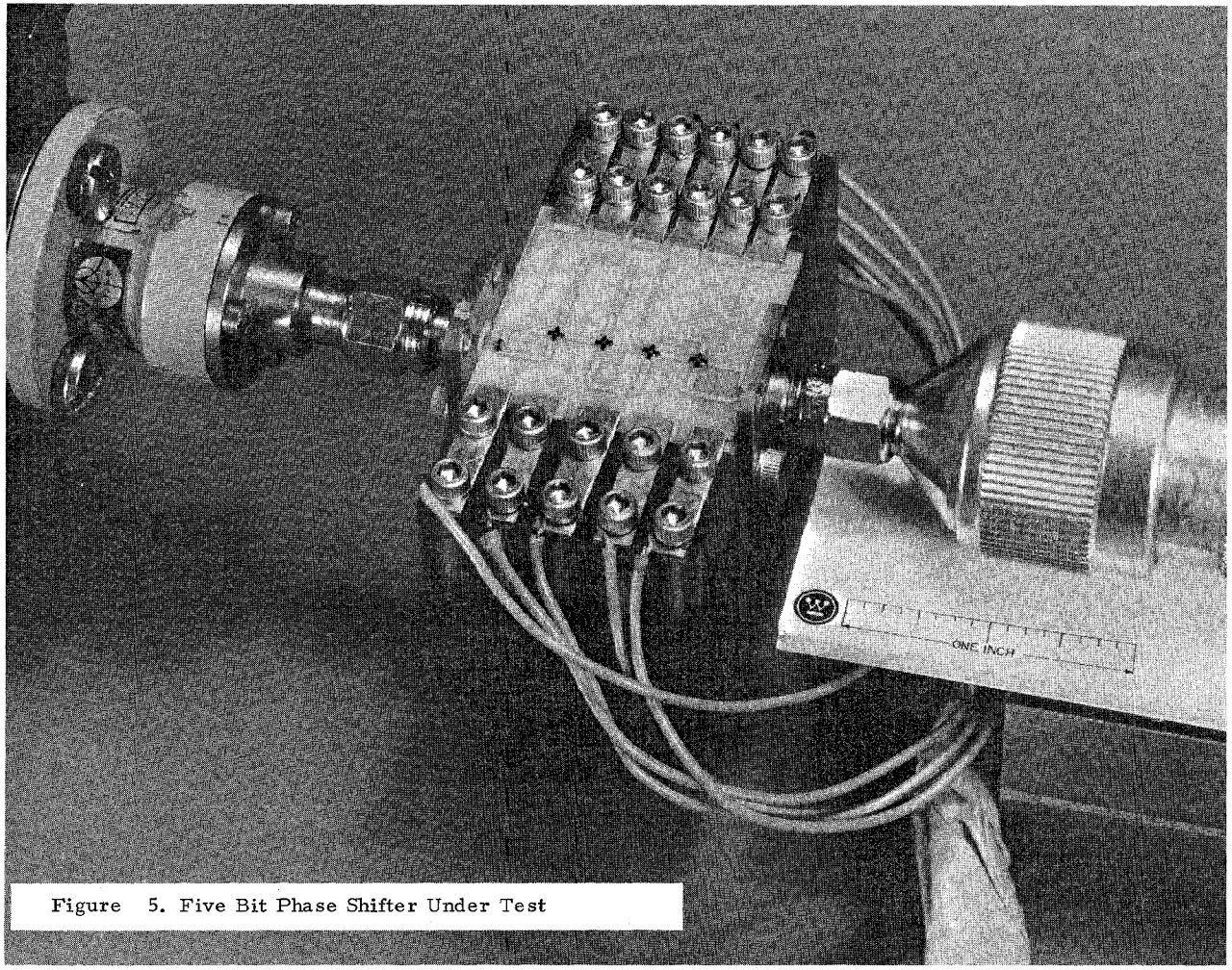

Figure 5. Five Bit Phase Shifter Under Test